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# Enhanced Skewed Load and Broadside Power Reduction in Transition Fault Testing

Mrs. A.Jyothi, Ms. P.Priyadharshika
1. Electronics and Communication Engineering, Arasu Engineering College, Kumbakonam , India
2. Electronics and Communication Engineering, Arasu Engineering College, Kumbakonam , India

**ABSTRACT**
This Paper Proposes the T-algorithm technique to optimize the testing Skewed Load and Broadside architecture. And the architecture used to the compare the test pattern results. In this architecture, T-algorithm used to optimize the testing architecture. This architecture compare the test pattern output for the required any type of combinational architecture. The optimization process mainly focused by gate optimization for secure architecture. The proposed system to use the T-algorithm, to optimize the testing clocking level for the required test patterns. This technique to replace the flip flop and the mux arrangement. To reduce the flip flops in Skewed Load architecture. And to develop the accuracy for testing architecture. The proposed system consists of the secure testing architecture and includes the XOR-gate architecture. So the modification process applied by the Broadside and over all Skewed Load architecture. The proposed technique to check the scanning results for the testing process. The testing architecture mainly used to the error attack for the scanning process and the scanning process work with any type of testing architecture. The scanning process to be secure using the T-algorithm for the Skewed Load architecture. And to develop the testing process for the fault identification process. The diagnosis technique to detect error for the scanning process in any type combinational architecture. The T-algorithm used to reduce the circuit complexity for the testing architecture and the testing architecture used to reduce the delay level. And the future process, this technique used to reduce the gate level for the sticky comparator architecture and to modify the clocking function for the testing process. This technique to develop the accuracy level for the testing process compare to the present methodology.
**Keywords**: Broadside Transition, Reduction of Flip-flops, Reduction of circuit complexity, Skewed Load, XOR gate Architecture

## I. INTRODUCTION

The SOC's test application time is major problem in Industries. The efficient way of reducing test application time for core based SOC's is, by ordering the tests concurrently. Several cores are tested at a same time. This, way of testing increases switching activity in chip,this results in higher power consumption. There exist a tradeoff between power consumption and testing time. By scheduling the modules, increases test time cost but reduces power consumption. The power model used often is global Peak Power Model where single power value, highest of power curve is used to represent power curves of each test. The advantage of this scheduling algorithm in test pattern has to keep track single value per test.

Significant researches efforts have been expended in reduce power dissipation during launch and capture cycle at speed testing. At the expense of pattern count inflation, the peak power is reduced. A partitioning approach has been proposed in where power wise costly patterns are further analyzed via fault simulation to identify the location of care bits, which dictate the partitioning of the design during capture; with few problematic patterns such an approach can deliver power savings. Partitioning the design and testing one partition at a time has been proposed to reduce launch and capture power in BIST.

## II. PROPOSED SYSTEM:

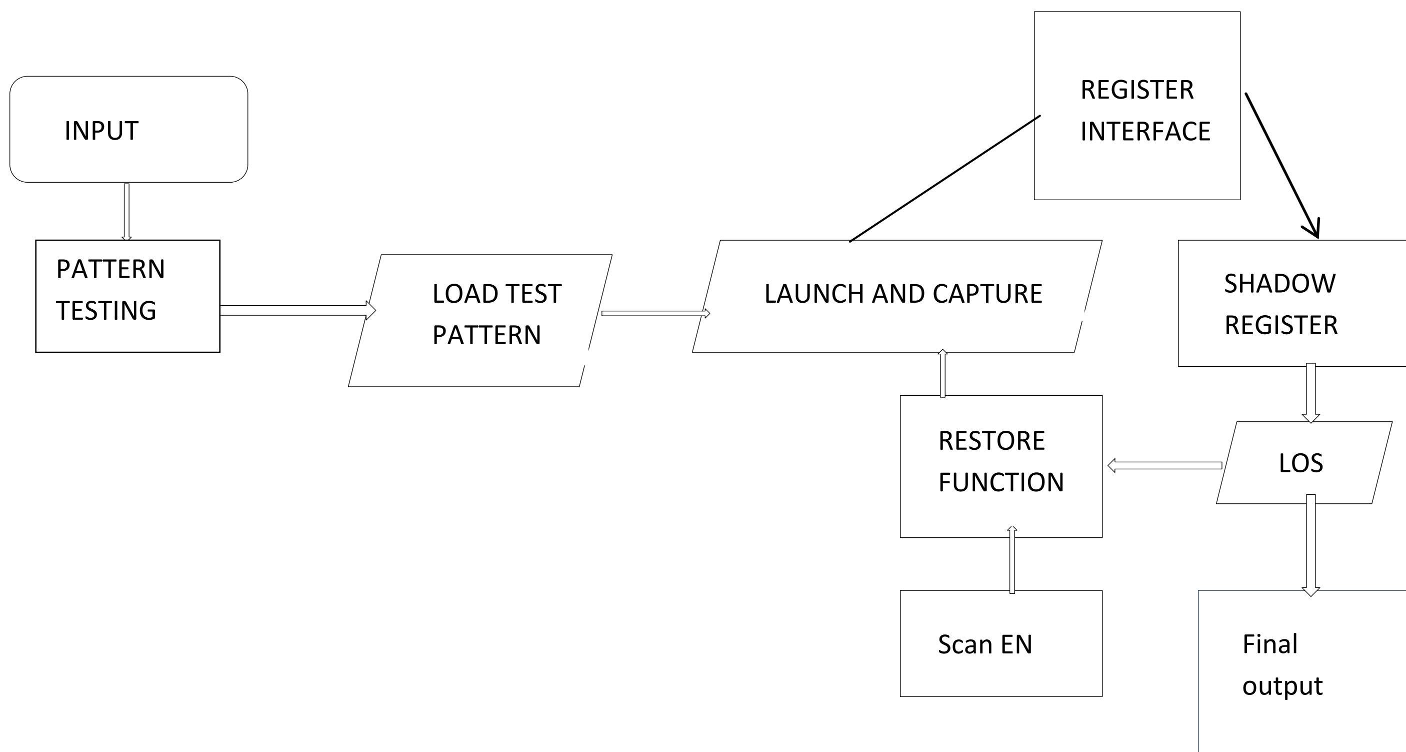
In skewed load and broadside transition, newly generated patterns aim for only one apportion at a time, this end up loading Interface registers of other partitions experiencing the penalty of test cost and data volume. Pattern count increases has been incurring even after the design is partitioned via ILP that minimizes capture violations. The proposed work is based on

T-algorithm based Enhanced Architecture. This algorithm optimizes scanning technology. This technique improves controllability of transition fault testing. Scan enable signal is not required to change at-speed. To identify the design regions, the s-graph is partitioned into strongly connected components. The SCC graph does not contain any cycles, delivers the acyclicity property of the graph. Acyclicity constraint still be met by merging operation of the cycle. Merging two operations of consecutive levels preserves the acyclicity of the graph; two regions

from the same level can also be merged without introducing any cycles

To restore the Load state of interface register upon launch and capture operations, one shadow test register is inserted for each interface register. The shift register copies the content of Interface register, and during capture window, the shadow register is not clocked,, assuring the copied value in last shift cycle is retained. The newly inserted logic falls on test paths only, incurring to test penalty. The total cost for $N_{int}$ interface registers is $N_{int}$ muxes and $N_{int}$+2 flip-flops

**BLOCK DIAGRAM:**




**LOAD STATE:**

First the given input test pattern for the launch and capture operation. So we load the test pattern into the scan cell, the load state to be arrange the test inputs. A test pattern may launch transition from a set of flip-flops which may possibly span multiple regions and capture these transitions in the region being tested. The challenge is that any test pattern may be testing any set of regions by launching transitions from any other set of regions.

**LAUNCH OFF CAPTURE**

The test pattern to apply the launch and capture process during the testing operation. To implement the launch off capture block into the load state. Region interface registers can be restored back to their load state upon launch and capture. DfT support that can restore the load state in interface registers in between the launch and capture operations in the design regions.

**REGISTER BLOCKS**

There are two register used in this architecture. Upon every launch and capture operation that the interface registers gets involved in it. Its load state is restored by copying the content of the shadow register back into the interface register. Throughout the shift operations, the shadow register copies the content of the interface register. Effectively, a multiplexer and a shadow flip-flop are inserted for the interface register, doubling the size of the interface scan cell.

**LAUNCH OFF SHIFT**

The test pattern to shift the next level using the Launch off Shift operation. As the LOS scheme launches transitions mainly followed by shift operation. The shadow registers can replace the bidirectional stitching for the restoration of the load state in LOS testing. A special stitching and the associated DfT support are required only for the

interface registers in order to enable a proper rewind operation.

## RESTORE FUNCTION

To restore the load state of the interface register upon the launch and capture operations. DfT support for the load state restores mechanism. Effectively, a multiplexer and a shadow flip-flop are inserted for the interface register, doubling the size of the interface scan cell. While the restore/rewind operations consume additional power. Our results show that this amount is always less than the power dissipated in the launch cycle, even after the launch power is reduced.

## SCHEMATIC DIAGRAM:

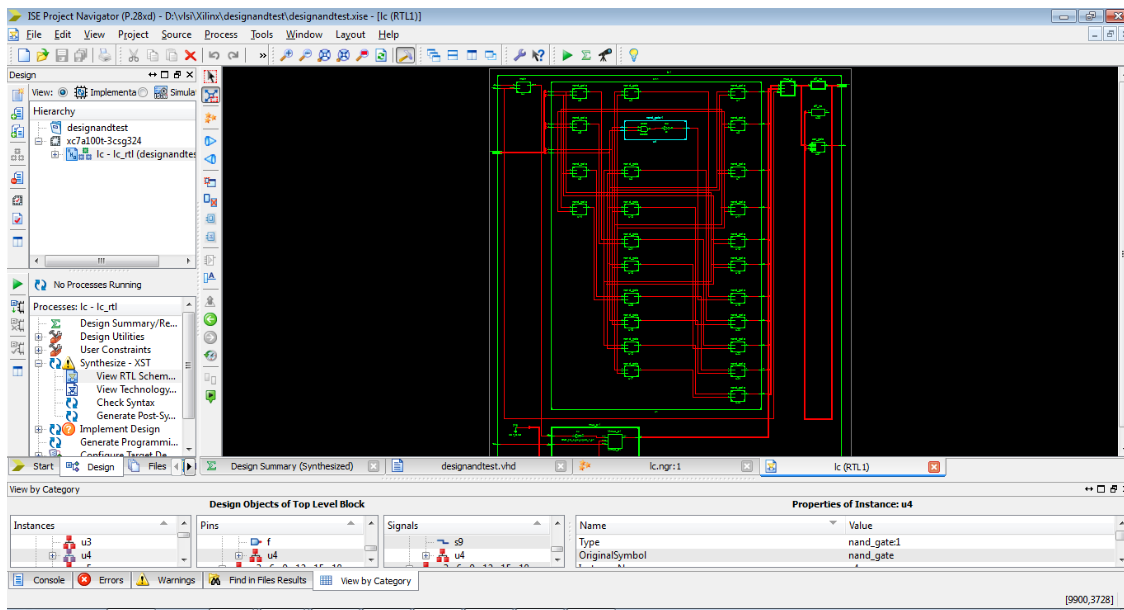



Figure 1

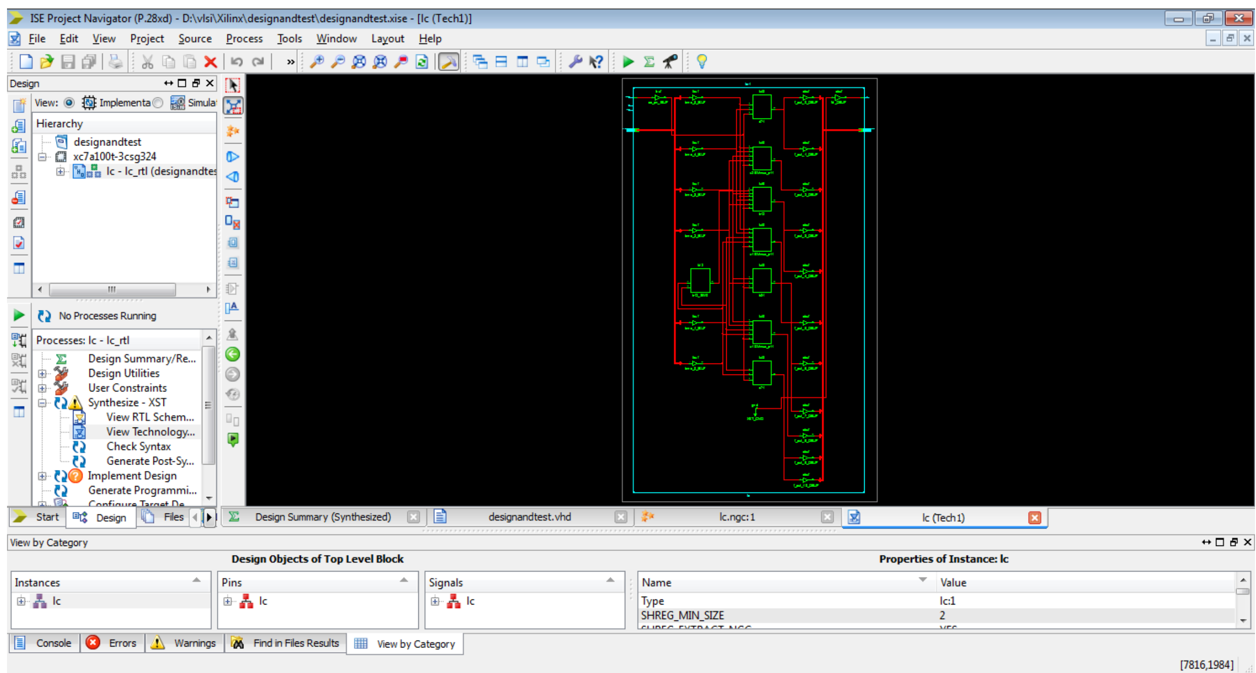



Figure 2

**OUTPUT:**

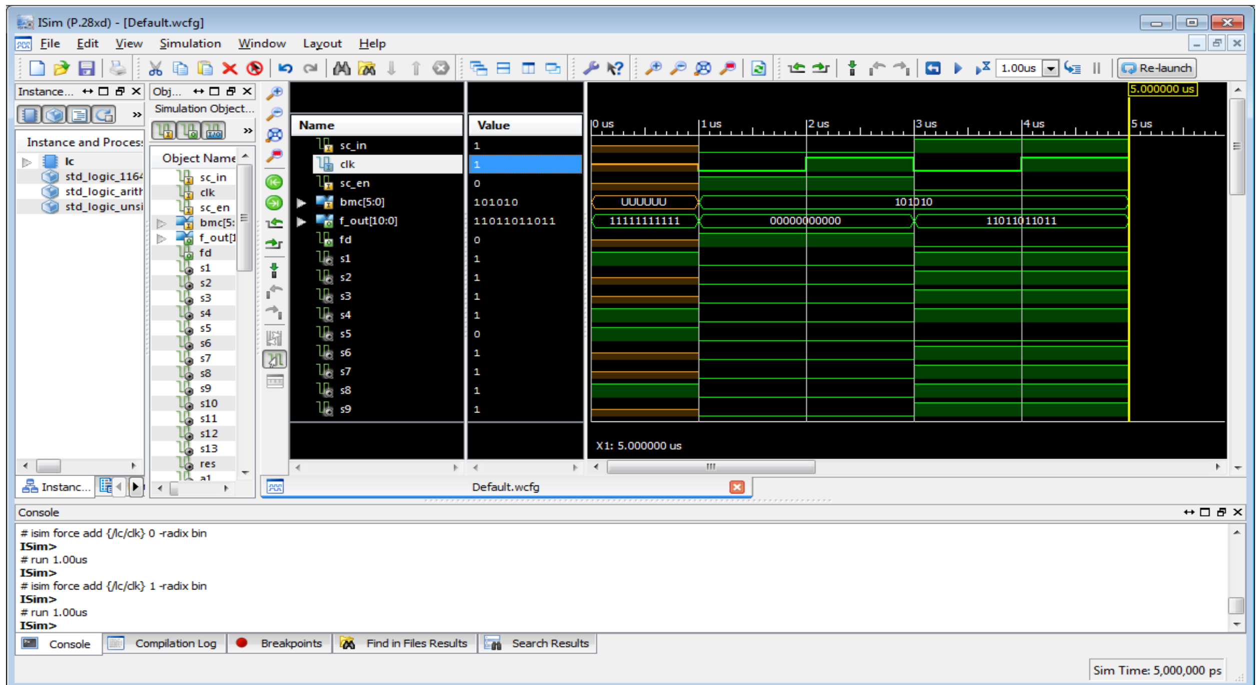



**Figure 3**

## COMPARISION TABLE:

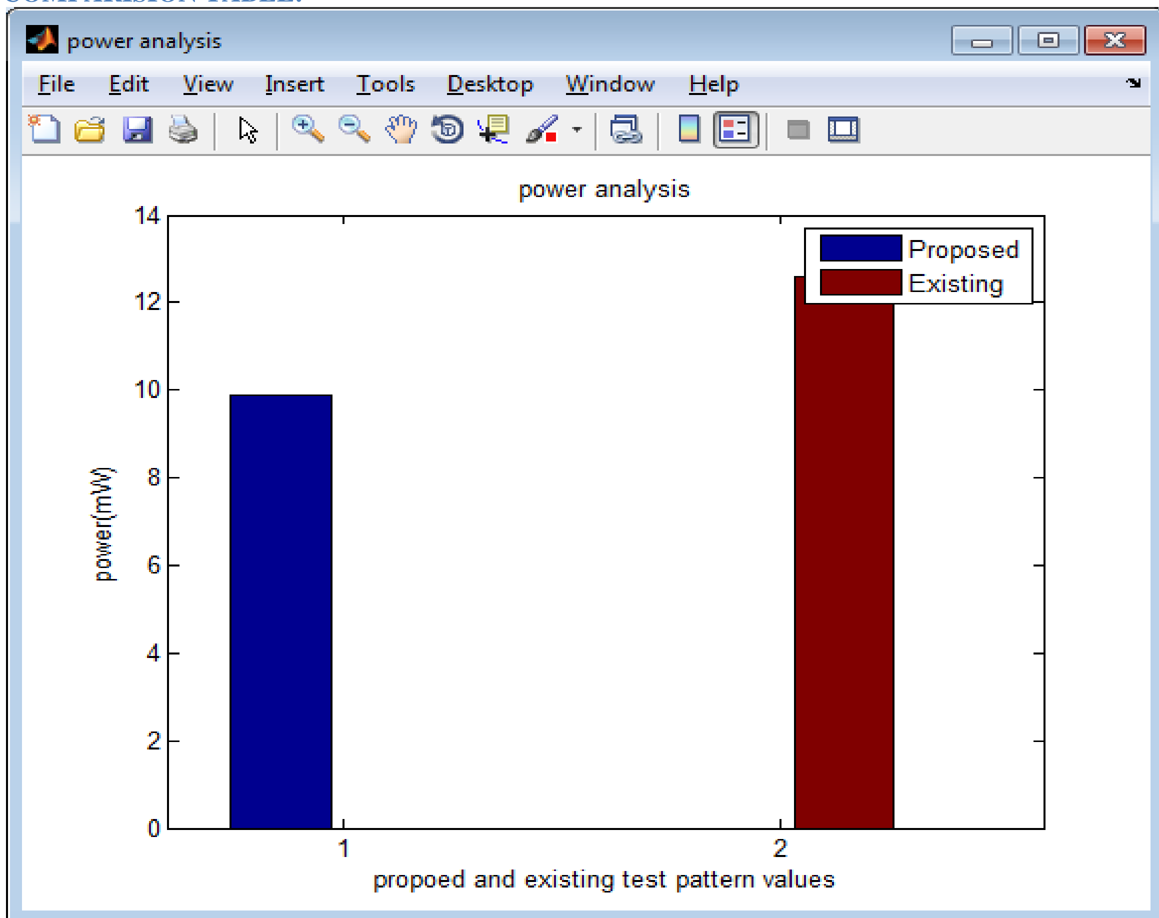



**Figure 4**

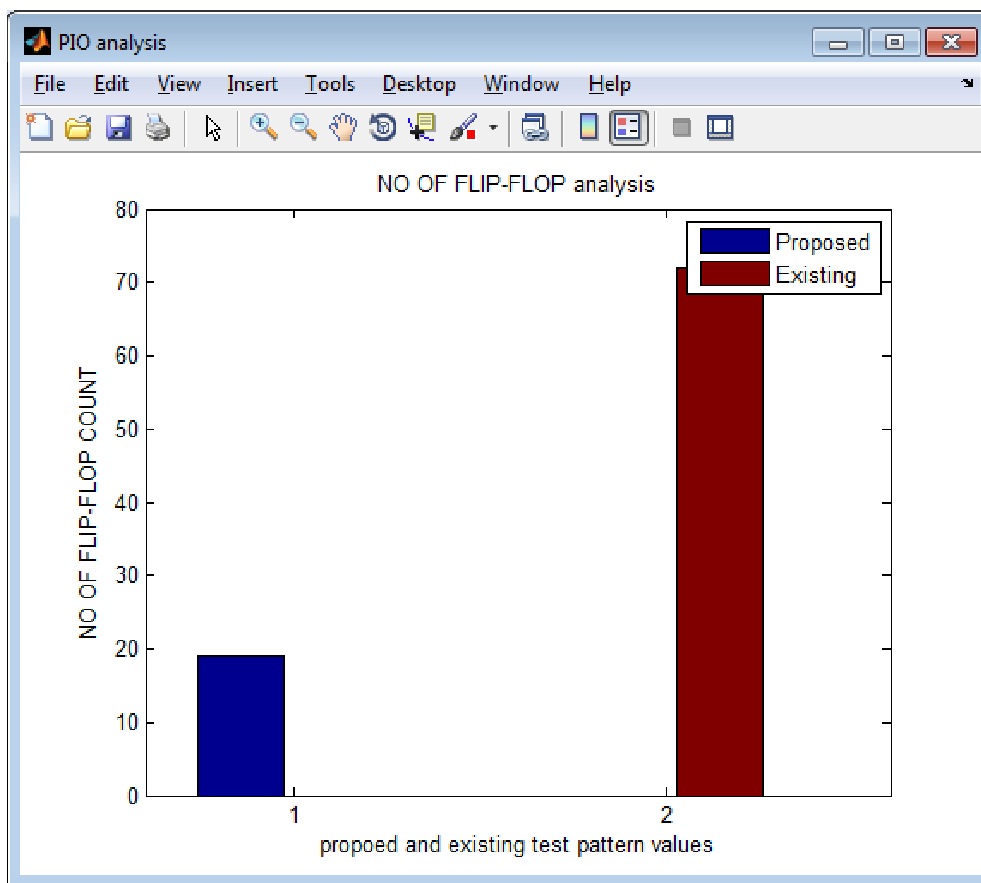



**Figure 5**

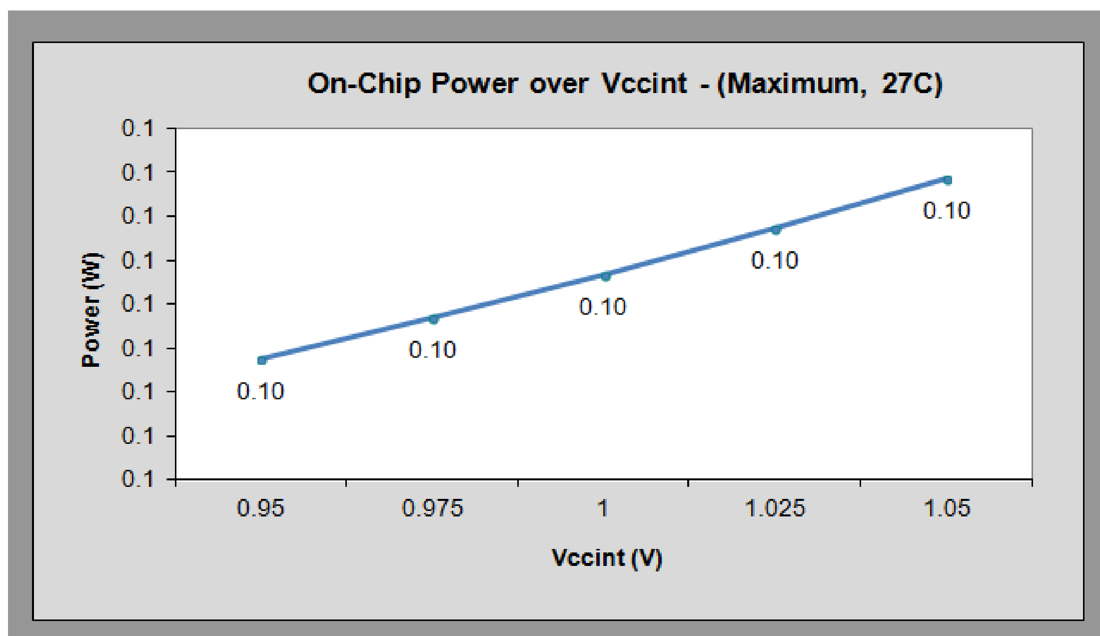



**Figure 6**

## III. CONCLUSION:

The increasing test application times for testing modular core-based SoCs can be minimized by concurrent execution of the tests. However, concurrent test application leads to higher power consumption, which must be taken into account in order to not violate the power constraint. The power consumption has previously been modeled as a single value per test. The power model takes the scan chain switching activity generated by the test stimuli and the test responses into account. Further, the model provides a separate power profile per wrapper chain configuration. We have implemented the power model and included it in anSoCtest scheduling algorithm. We have made extensive experiments on several ITC'02 benchmarks and an industrial design, where we compare the testing time when using a single-value (global peak) power model and the proposed cycle-accurate power model.

We proposed DfT support that can restore the load state in interface registers in between the launch/capture operations in the design regions, enabling low-power LOC, LOS, and mixed at-speed testing. This way, a set of patterns optimized for cost and quality can be utilized as is, yet in a low power manner.

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